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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,525	03/29/2004	Stephen M. Trimberger	X-1006-2C US	3296
24309	7590	09/02/2005	EXAMINER TAN, VIBOL	
XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124			ART UNIT 2819	PAPER NUMBER

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/812,525

Applicant(s)

TRIMBERGER, STEPHEN M.

Examiner

Vibol Tan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 13-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2 and 7-16 is/are allowed.
- 6) ☒ Claim(s) 3-6,17-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 3-6 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Selvidge et al. (U. S. PAT. 5,850,537).

In claim 3, Selvidge et al. teaches all claimed features in Fig. 3 an integrated circuit comprising: a set of configurable logic blocks (22s inside 12) comprising multiple signal sources (24a-24d) and at least one destination (12'); a time multiplexing signal generator (col. 5, line 50; time division multiplexed) controlling which of the multiple signal sources provides its signal to a corresponding signal destination (12'); and a programmable interconnect (14) coupled between an output (26) of the time multiplexing signal generator and a destination configurable logic block.

In claims 4-6, Selvidge et al. further teaches the integrated circuit of Claim 3, wherein the multiple signal sources are located in one configurable logic block (22); wherein the multiple signal sources generate critical signals (col. 14, lines 15 and 30)., and wherein the time multiplexing signal generator includes a counter (col. 13, line 11).

In claim 17, Selvidge et al. further teaches the integrated circuit of Claim 3, further comprising a plurality of destinations (24'a-24'd) within the destination configurable logic block, wherein the signal source of the multiple signal sources

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selected by the time multiplexing signal generator (405 in Fig. 7A) is coupled to one of the destinations within the destination configurable logic block.

In claims 18-20, Selvidge et al. further teaches the integrated circuit of Claim 3, further comprising a plurality of destination configurable logic blocks (within 12'); wherein the time multiplexing signal generator comprises a multiplexer (405) coupled to the multiple signal sources and controlled by a time multiplexing signal (Sel); and wherein each destination configurable logic block comprises a capture device (I₁) coupled to receive the time multiplexing signal, wherein at least one configurable logic clock is coupled to receive a signal from the selected signal source based upon the time multiplexing signal.

3. Claims 1, 2 and 7-16 appear to comprise allowable subject matters.

Response to Arguments

4. In view of further consideration the new ground(s) of rejection has been set forth, as discussed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).



VIBOL TAN
PRIMARY EXAMINER